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IP CORES GENERATORS IN SOC DESIGN

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ABSTRACT

Newest INTRON IP Cores Generator creation methodology, which allows generating optimized IP Cores on base of scalable source IP modules, is presented. As examples, INTRON's Fast Fourier Transform IP Cores Generator and Data Encryption Standard IP Cores Generator are presented.

Keywords: IP Cores, SoC Design, IP Core Generators.

1. INTRODUCTION

Recent years have seen impressive improvements in the achievable density of integrated circuits. In order to maintain this rate of improvement, designers need new techniques to handle the increased complexity inherent in these large chips. One such emerging technique is the System-on-a-Chip (SoC) design methodology [1, 2]. In this methodology, pre-designed and pre-verified blocks, often called *cores* or *intellectual property (IP*) [3, 4], are obtained from internal sources or third parties, and combined onto a single chip. These cores may include embedded processors; memory blocks, or circuits that handle specific processing functions. The SoC designer, who would have only limited knowledge of the structure of these cores, could then combine them onto a chip to implement complex functions.

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2. SOC-STYLE DESIGN

Figure 1 shows a hypothetical SoC-style design containing a programmable logic core. The chip consists primarily of fixed function IP Cores, likely obtained from a third-party.

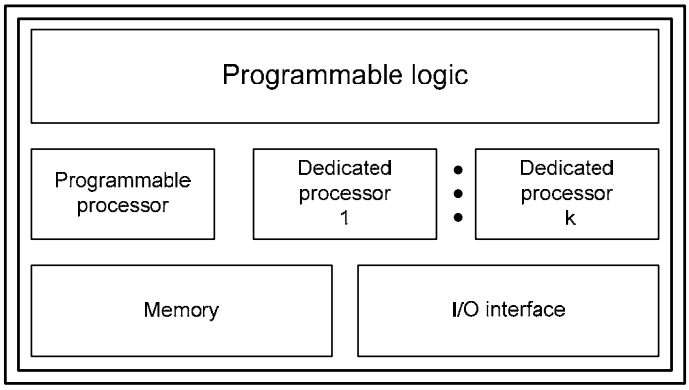

Fig.1. A hypothetical SoC-style design containing a programmable logic core.

In this particular example, the fixed cores include an embedded programmable processor, some on-chip memory, and *k* other fixed-function cores (dedicated processors). In addition, the chip contains a programmable logic core. Unlike the other cores the functions implemented by the programmable logic core need not to be defined before the chip is fabricated. Also, the programmable logic core contains a set of uncommitted gates surrounded by a set of programmable interconnects.

Thus the user has a possibility to complete the SoC's functionality in appropriate way by programming a programmable logic core already after the chip is fabricated (see Figure 2).

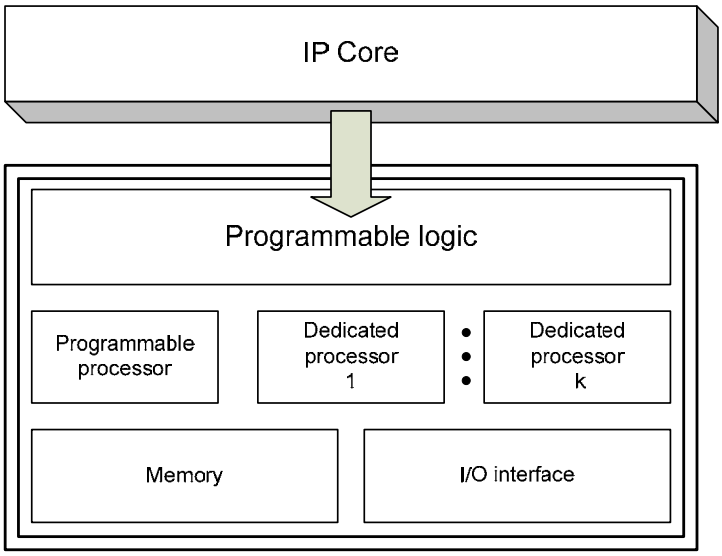

Fig.2. SoC completion after the chip fabrication.

3. IP CORES GENERATORS

SoC design enters into mainstream usage. The ability to make system unit's functions and parameters selection and their post-fabrication changes becomes more and more attractive. This ability can be realized using IP Cores Generators [5, 6].

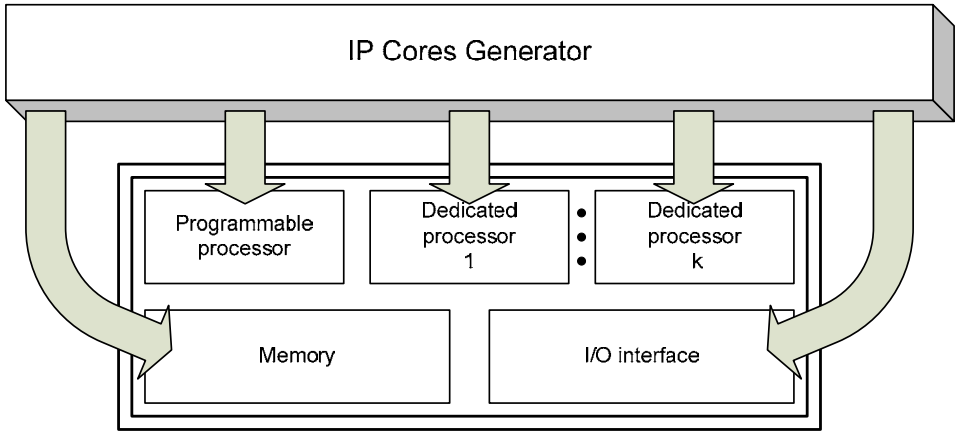

Fig.3. IP Cores Generator-based SoC design.The IP Core Generator is a high-level software tool, which allows obtaining an IP Core with required characteristics

automatically. These IP Cores Generators are used for IP Cores generation before SoC design or when it is needed to change its functions after fabrication (see Figure 3).

4. IP CORE GENERATION USING SCALABLE PARAMETERIZABLE VHDL-MODEL

The INTRON IP Core Generators methodology allows generating optimized IP Cores on a base of scalable IP modules' source. The Generator produces target VHDL description of IP Core on a base of scalable IP Core architecture template. The IP Core architecture is presented as scalable parameterizable description of target IP Core architecture. True configuration makes possible the effectively using of the resources of available hardware. It's achieved by precision optimization of all parts of IP Core by Generator. Also the IP Core Generator generates test bench with test patterns (see Figure 4).

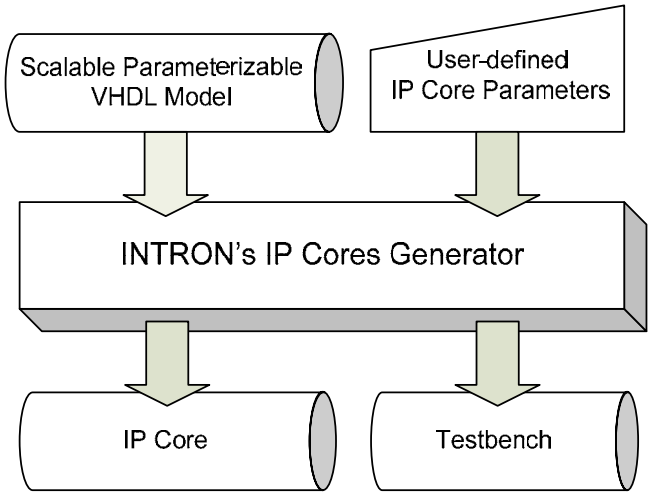

Fig.4. Technique of INTRON's IP Core Generator.

5. IP CORES GENERATORS SAMPLES

Using proposed methodology, INTRON's Fast Fourier Transform IP Cores Generator and Data Encryption Standard IP Cores Generator were created.

The INTRON's Fast Fourier Transform (FFT) IP Cores Generator [7] is intended for generation a fully optimized FFT Processor architecture and test bench with test patterns according to user-defined parameters (see Table 1). The FFT Processor computes the N-point complex direct or inverse FFT. The input (output)

data is a vector of N complex values represented as 2's complement numbers – real and imaginary components of a data sample. The input data stream is represented in natural order, output in binary-inverse order. Using proposed FFT Processor IP Core Generator on Altera's FPGA, several kinds of FFT Processors were generated and implemented. Implementation results are summarized on Table 2.

Table 1. Fast Fourier Transform IP Cores Generator Parameters

Parameter	**Description**
FFT Size	Number of points, must be power of 2.
FFT External Wordwidth	Wordwidth of each input real and imaginary part of complex data
FFT Internal Wordwidth	Wordwidth of sine and cosine coefficients, wordwidth of internal data.
Transform Type	Direct or Inverse.
Test Patterns	Test patterns number, skip test bench if 0.

Table 2. FFT Processors sample realization on Altera APEX20KE FPGA

Parameters	**Characteristics**
16-point FFT, 16-bit ext. datawidth, 20-bit internal datawidth	Utilization - 6432 LE. Fmax - 72,4 MHz. Performance - 2,31 Gbit/s. Transform Time - 220 ns. Pipeline Delay -855ns.
64-point FFT, 24-bit ext. datawidth, 32-bit internal datawidth	Utilization - 35117 LE. Fmax - 39,04 MHz. Performance - 1,87 Gbit/s. Transform Time - 1,639 us. Pipeline Delay -4,559 us.
1024-point FFT, 16-bit ext. datawidth, 20-bit internal datawidth	Utilization - 35982 LE, 69504 ESB. Fmax - 65 MHz. Performance - 2,08 Gbit/s. Transform Time - 15,749 us. Pipeline Delay - 33,128 us.
8192-point FFT, 4-bit ext. datawidth, 8-bit internal datawidth	Utilization - 20383 LE, 181888 ESB. Fmax - 100,1 MHz. Performance - 800 Mbit/s. Transform Time - 81,912 us. Pipeline Delay -165,263 us.

The INTRON's Data Encryption Standard IP Cores Generator was created according to analysis of possible DES and Triple DES Processors architectures and singling out the expedient for realization their variations [8, 9]. Selected parameters are described on Table 3. Results of synthesis of some representative samples are summarized on Table 4.

Table 3. Data Encryption Standard IP Cores Generator Parameters

Parameter	Description
Algorithm of the data encipherment	DES, Triple DES.
Mode of the block ciphers work	ECB, CBC, CFB, OFB.
Encipherment direction	Encryption, decryption, encryption and decryption.
Processed data blocks size	1 bit, 64 bits.
Architecture of the processor core	Iterative, pipelined.

Table 4. DES and Triple DES Processors sample realization on Altera STRATIX II FPGA

Parameters	Characteristics
64-bit ECB DES Processor with iterative architecture	Utilization – 383 ALUTs. Fmax - 238,10 MHz. Performance - 952,4 Mbit/s. Encryption Time – 67,2 ns.
64-bit ECB DES Processor with pipelined architecture	Utilization – 2655 ALUTs. Fmax – 253,87 MHz. Performance – 16247,68 Mbit/s. Encryption Time – 3,939 ns. Pipeline Delay - 63,024 ns.
64-bit ECB Triple DES Processor with iterative architecture	Utilization – 590 ALUTs. Fmax – 183,28 MHz. Performance - 244,38 Mbit/s. Encryption Time – 261,89 ns.
64-bit ECB Triple DES Processor with pipelined architecture	Utilization – 10965 ALUTs. Fmax – 182,05 MHz. Performance – 11651,2 Mbit/s. Encryption Time – 5,50 ns. Pipeline Delay -263,664 ns.

6. CONCLUSIONS

Due to strict requirements of time-to-market the technologies of IP Cores generators development and their wide usage becomes more and more attractive. Over 10 years INTRON Ltd. focuses on designing of configurable and reconfigurable architectures of specialized processors and techniques of their creation. Since some years these works result on creation of IP Cores Generators. High technical characteristics of represented in this paper generated IP Cores indicate the expedience of wide application of IP Cores generators in IP Cores and SoC market. It is a write way to reduce chip's time-to-market and to satisfy more customers' requirements.

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