RGB2YUV Color Space Converter IP Core

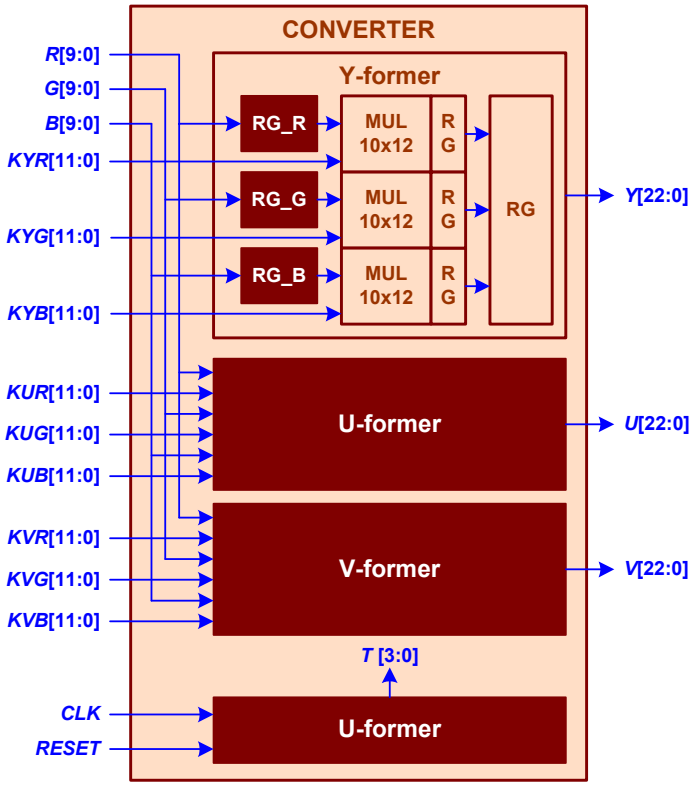
General information

Luminance and color difference coded signals (YUV) are used by many component video systems. Conversion from RGB is necessary to feed a device requiring YUV input.

Features

- *Converts digital RGB to digital component video YUV;*
- *Optimized for XC4000XLA and Virtex architecture;*
- *Low CLB count/MIPS ratio;*
- *Supports camcorder video streams;*
- *Up to 56 MHz System clock;*
- *Up to 14 MHz RGB change;*
- *One conversion per 8-clock cycle;*
- *All outputs no rounded;*
- *No external logic needed to handle these conditions;*
- *Low latency;*
- *Fully relationally placed for consistent performance;*
- *Supports Xilinx Foundation Series 2.1i development tools.*

RGB2YUV IP Core pinout



Functional description

The RGB to YUV color space converter is designed to perform the following equations:

Y = + KYR*R + KYG*G + KYB*B

U = - KUR*R - KUG*G + KUB*B + C1

V = + KVR*R - KVG*G - KVB*B + C1

R, G, B – are 10 bit values;

K – are 12 bit values;

Y, U, V – are 23 bit positive values;

C1 – a constant.

The conversion is complete in 8 clock cycles and both input and output are registered for consistent routing and timing.

Multipliers

These multipliers are high speed recursive implementations that multiply a 10-bit wide variable by a 12-bit variable and produce a 22 bit wide result. The 10x12 multiplier is built on the base of 10x3 multipliers.

Limiting

The limiting function protects against negative results for U and V.

The 4194303 offsets is added for U and V equations:

Y = + KYR*R + KYG*G + KYB*B

U = - KUR*R - KUG*G + KUB*B + 4194303

V = + KVR*R - KVG*G - KVB*B + 4194303

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Interface description

Pin	Activity	Description
CLK	Positive clock edge	Clock
RESET	HIGH	Synchronous Reset
Y[22:0]	-	Luminance
U[22:0]	-	U
V[22:0]	-	V
R[9:0]	-	Red
G[9:0]	-	Green
B[9:0]	-	Blue
KYR[11:0]	-	Coefficient for Y and Red
KYG[11:0]	-	Coefficient for Y and Green
KYB[11:0]	-	Coefficient for Y and Blue
KUR[11:0]	-	Coefficient for U and Red
KUG[11:0]	-	Coefficient for U and Green
KUB[11:0]	-	Coefficient for U and Blue
KVR[11:0]	-	Coefficient for V and Red
KVG[11:0]	-	Coefficient for V and Green
KVB[11:0]	-	Coefficient for V and Blue

Sample implementation

Device Family	XC4085XLA	Virtex XCV400
CLBs (Slices) Used	534	(483)
IOBs Used	207 *1)*	207 *1)*
CLKIOBs Used	1	1
System Clock f max	56 MHz	60 MHz
Device Features Used	Fast Carry Logic	Fast Carry Logic
Design File Formats	Foundation Series 2.1i	Foundation Series 2.1i
Constraint Files	Yes	Yes
Verification Tool	Foundation Series 2.1i	Foundation Series 2.1i
Schematic Symbols	Foundation Series 2.1i	Foundation Series 2.1i

1) Assuming all core signals are routed off-chip.

Design tool requirements

Tool	Version
Xilinx Core Tools	Foundation Series 2.1i
Entry/Verification Tool	Foundation Series 2.1i

Verification methods

The core has been tested with in-house developed test vectors that are provided with the core. The pinout of the color space converter has not been fixed to specific FPGA I/O, allowing flexibility with a user's application.

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