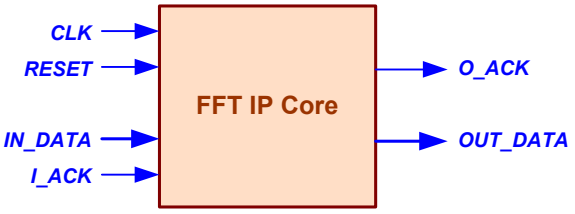
Direct and Inverse Fast Fourier Transformations IP Cores

Features

- *Any radix-2 length direct or inverse FFT;*
- *Fixed complex I/Os with any width;*
- *Arbitrary width of the internal data and coefficient word;*
- *No external memory required;*
- *Fixed-point arithmetic;*
- *Simple interface and timing;*
- *No dead clock cycles;*
- *Fully pipelined structure, fully synchronous;*
- *Registered Inputs and Outputs;*
- *Full test bench supplied;*
- *Natural order input, binary-inverse output.*

FFT IP Core pinout



General information

The FFT Processor computes the N-point complex direct or inverse FFT. The input (output) data is a vector of N complex values represented as 2's complement numbers – real and imaginary components of a data sample. The input data stream is represented in natural order, the output – in binary-inverse order.

The FFT IP Cores are generated automatically using the INTRON's FFT IP Cores Generator, which is intended to generate fully optimized FFT Processor's architecture and optional test-bench with test patterns. INTRON's FFT IP Cores Generator is based on newest INTRON IP Core Generator's methodology, which allows generating optimized IP Cores on a base of the scalable source IP modules.

FFT IP Cores parameters

Parameter	Description
FFT size	Number of points, must be a power of 2
FFT external word width	Word width of each input real and imaginary part of complex data
FFT internal word width	Word width of sine and cosine coefficients, word width of internal data
Transformation type	Direct or inverse
Test patterns (optional)	Test patterns number

Sample implementations

Device: Altera Apex 20KE	Utilization	Performance	Transformation time*	Pipeline Delay	Synthesis and implementation tools
16-point FFT, 16-bit ext. datawidth, 20-bit internal datawidth					
EP20K200EQ240-1x	6432 LE 0 ESB	72,4 MHz 2,31 Gbit/s	220 ns	855ns	Synplify, Altera
64-point FFT, 24-bit ext. datawidth, 32-bit internal datawidth					
EP20K1500EBC652-1	35117 LE 0 ESB	39,04 MHz 1,87 Gbit/s	1,639us	4,559us	Synplify, Altera
1024-point FFT, 16-bit ext. datawidth, 20-bit internal datawidth					
EP20K1500EBC656-1x	35982 LE 69504 ESB	65 MHz 2,08 Gbit/s	15,749us	33,128us	Synplify, Altera
8192-point FFT, 4-bit ext. datawidth, 8-bit internal datawidth					
EP20K1500EBC652-1	20383 LE 181888 ESB	100,1 MHz 800 Mbit/s	81,912us	165,263us	Synplify, Altera

* Transformation time = N / Fmax.

Altera – Altera Quartus II version 1.1 build 155;
Synplify – Synplicity Synplify VHDL Compiler, version 6.2.4.

At your request we can generate or/and modify the core to meet your specific requirements.

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